REMARKS

Favorable reconsideration and allowance of the subject application are respectfully requested. Claims 1-26 are pending in the present application, with claims 1, 6, 9, 14, 19, and 22 being independent.

Specification

The Examiner objected to paragraph 0012 of the specification. Specifically, the Examiner questions if the counter should be reset before applying the clock phase and that if the counter is reset after applying the clock that the counter will not provide a measure of the clock phase because the counter will be forced to a predetermined state.

First, Applicants respectfully submit that the feature of "resetting" of a counter is disclosed at least in Fig. 17 and on pages 27-28 of the present application. Referring to these cited sections, one skilled in the art would understand that a sampling clock signal is provided from a primary clock source 140 operating at a frequency f. A sub-sampling clock source 142 as a secondary clock operates at a multiple of the primary clock 140, such as 100f. The sub-sampling source clock 142 clocks a counter 144 that has values 0-99, for example, and is reset by pulses from the primary clock 140. Thus, the numeric count in the counter 144 indicates a sub-sample time value in hundredths of a sample interval.

For example, counter 144 starts with a value of "0" and is incremented up to "99" driven by the secondary clock. As the sub-sampling rate of the secondary clock is a hundred times higher than the sampling rate of the primary clock a sampling interval covers one sub-sampling cycle with 100 steps from "0" to "99." Therefore, the counter provides a measure of the clock phase, as indicated in

Fig. 17 by line 146, by sub-dividing each sampling interval. Due to the triggering by the sample clock, the counter is correlated and synchronous. Thus the counter provides a measure of the clock phase.

Accordingly, in view of the above comments, withdrawal of the objection is respectfully requested.

Claim Objections

The Examiner objected to claims 2, 6-8, and 19-21 because of minor informalities. Applicants have amended the claims in an effort to correct these minor informalities. Furthermore, Applicants respectfully submit that these amendments do not narrow the scope of the claims.

With respect to independent claims 6 and 19, Applicants have amended these claims to clarify that a desired signal is generated based on the measure of clock phase derived from the sub-sample clock signals. Applicants respectfully submit that this amendment does not narrow the scope of the claims and was merely made in an effort to clarify the features therein.

Accordingly, withdrawal of the objections is respectfully requested.

Drawings

The Examiner objected to the drawings stating that the following features, recited in claim 9, must be shown:

> - determining in the receiver a frequency difference between the received code rate and the locally generated code rate; and
> - applying the frequency difference to the locally generated code rate to provide an adjusted locally generated code rate.

Applicants respectfully submit that these features are shown in, at least, Fig. 16, which is a block diagram of a generalized signal processor in which it is desired to sample periodic signals received at a nominal frequency f over a line 130, using a local clock source 132. The sampling frequency is assumed to be a multiple of, and derived from, the local clock frequency. There is a frequency difference or error, designated e, between the incoming signal frequency and the local clock frequency (i.e., "between the received code rate and the locally generated code rate"). For purposes of illustration, the received Signals are assumed to be at frequency f and the local clock source 132 generating signals at a frequency (f+e). The frequency error e may be due to movement of the received signal source, a real error in the local clock source frequency, or a deliberately introduced error in the local clock source frequency. The error frequency measurement is determined in a frequency difference determination circuit 134 (i.e., "determine in the receiver a frequency difference between the code rate and the locally generated code rate"). This may be, as in the GPS receiver case, an adder that integrates received frequency measurements at a rate derived from the local clock source 132. The circuit 134 provides an output at a frequency proportional to the error frequency e. A frequency adjustment circuit 136 compensates for the frequency error and provides a clock signal at frequency f, to be used in demodulation of the received signals (i.e. "applying the frequency difference to the locally generated code rate to provide an adjusted locally generated GPS code rate"). Thus, all of the features of claim 9 are shown in the drawings.

Regarding claim 10, the Examiner states that following features must be shown:

> -the step of applying the frequency difference to the locally generated code includes dividing the frequency difference by a selected value, using a counter to provide an output signal whenever the counter overflows, to indicate that the frequency difference has resulted in a cumulative phase error equivalent to a code rate period; and

-the step of deriving a code phase value includes multiplying the code rate period by the ratio of the current counter contents to a counter value.

Again, Applicants respectfully submit that these features are shown in at least Fig. 15. Referring to Fig. 15, there are shown several circuits for dividing signals, e.g., a divide-by-77 circuit 120, a divide-by-3/4/5 circuit 122, and a divide-by-10 circuit 124. The circuit 120 receives, over line 42, a signal that varies at a rate related to the frequency derived from the phase loop. This signal is derived as one of the bits of the adder and register/latch 100 that represents a frequency of 616d, where d represents the Doppler (and other frequency error) component of the received signal frequency. Although d is referred to as the scaled Doppler frequency, it is taught in the specification that the term Doppler is also used to encompass other inevitable differences between a received signal frequency and the locally generated clock source of the same nominal frequency. Therefore, this frequency difference is fed to a divider circuit.

Regarding claim 21, Applicants respectfully submit that the unit for applying, the unit for resetting and the unit for using, are shown in at least Fig. 17, namely they are represented by box 144. Referring to Fig. 17, it can be readily seen that the incoming clock signal is for applying the sub-sample clock signals; the incoming reset is used for resetting; and the outgoing line 146 is for using the counter value as the measure of clock phase. Thus, although box 144 does not have individual boxes drawn depicting each unit, box 144 generally depicts these items such that one skilled in the art would understand. Therefore, all of the features of claim 21 are shown in the figures.

Accordingly, in view of the above comments, withdrawal of the drawing objection is respectfully requested.

Conclusion

In view of the above amendments and remarks, this application appears to be in condition for allowance and the Examiner is, therefore, requested to reexamine the application and pass the claims to issue.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Martin Geissler (Reg. 51,011) at telephone number (703) 205-8000, which is located in the Washington, DC area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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